Switching Characteristics of devices

Diode as a switch : Electronic devices such as junction diodes, transistors and vaccum tubes all have extreme regions of operation in which they nominally do not conduct even when large voltages are applied and there are regions in which they nominally do not conduct heavily even when relatively small voltages are applied. In the first of these regions, the device is described as being open and off or nonconducting. In the other extreme region the device is described as being ON, closed or conducting. When the device is driven from one extreme condition to the other, it operates as a switch.

Piecewise Linear diode characteristics :

This is a way to approximate the V-I characteristics of a diode using only straight lines i.e linear relationships. In such approximation, the diode forward resistance is neglected and the diode is assumed to conduct instantaneously when applied forward biased voltage v_D is equal to cut-in voltage V_γ. and then it is assumed that the current increases instantaneously giving straight line nature of V-I characteristics. while in reverse biased condition $V_D < 0$, the diode does not conduct at all.

When the transistor acts as a switch, it is either in cut-off or in saturation. To consider the behaviour of the transistor as it makes transition from one state to the other, consider the circuit shown in fig(a) driven by the pulse shown in fig(b). The pulse waveform makes transitions between the voltage levels V_1 and V_2. At V_2 the transistor is at cutoff and at V_1 the transistor is in saturation. The i/p waveform v_i is applied between the base and the emitter through a resistor R_B.

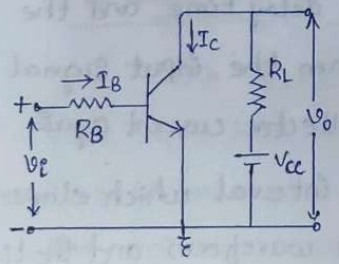
The response of the collector current I_c to the input waveform, together with its time relationship to that waveform is shown in fig(c). The collector current does not immediately respond to the input signal. Instead there is a delay and the time that elapses during this delay, together with the time required for the current to rise to 10% of its maximum value ($I_{cs} = V_{cc}/R_c$) is called the "delay time t_d". The current waveform has a non zero rise time 't_r' which is the rise time required for the current to rise from 10% to 90% of I_{cs}. The total turn-on time t_{ON} is the sum of the delay time and the rise time i.e "$t_{ON} = t_d + t_r$". When the input signal returns to its initial state, the collector current again fails to respond immediately. The interval which elapses between the transition of the input waveform and the time

** The region below the $I_B = 0$ curve is the cut-off region. the intersection of the load line with $I_B = 0$ curve is the "cut-off point". At this point, the base current is zero and the collector current is negligible. The emitter diode comes out of forward bias and the normal transistor action is lost i.e $V_{CE(cutoff)} \approx V_{cc}$. The transistor appears like an open switch.

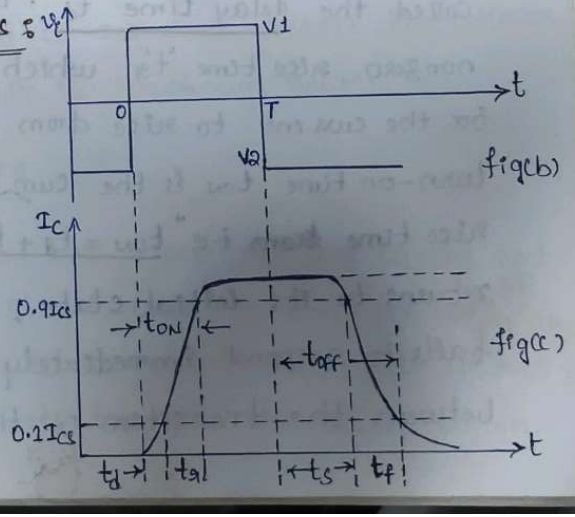
** The intersection of the load line with $I_B = I_{B(sat)}$ curve is called the "saturation point". At this point, the base current is $I_{B(sat)}$ and the collector current is maximum. At saturation the collector diode comes out of cut-off and again the normal transistor action is lost i.e $I_{C(sat)} = V_{cc}/R_L$.

** for $0 < I_B < I_{B(sat)}$, the transistor operates in the "active region", If the base current is greater than $I_{B(sat)}$ the collector current approximately equals to V_{cc}/R_C and the transistor appears like a closed switch.

Transistor Switching times :



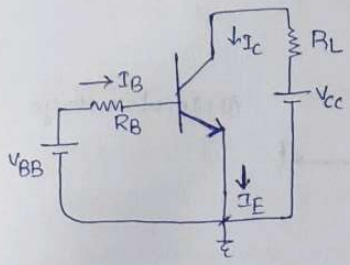
fig(a)

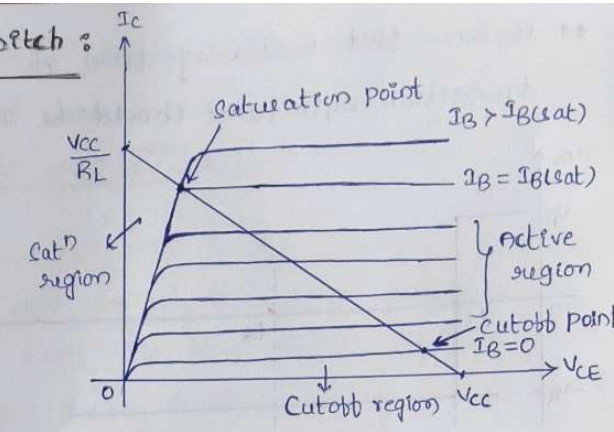


fig(b)

fig(c)

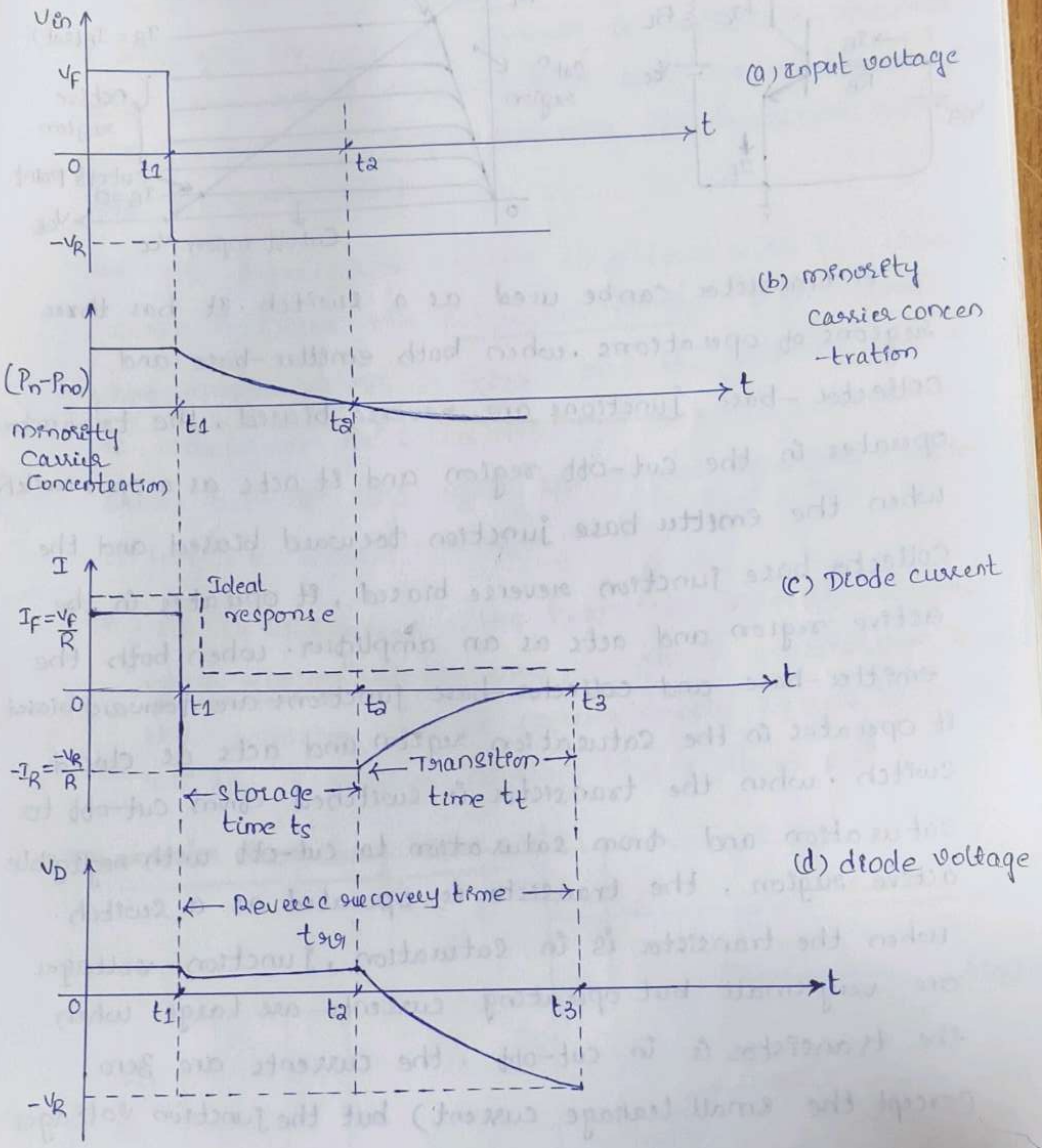
Transistor as a switch :





A transistor can be used as a switch. It has three regions of operations. when both emitter-base and collector-base junctions are reverse biased, the transistor operates in the cut-off region and it acts as a open switch. when the emitter base junction foreward biased and the Collector base junction reverse biased, it operates in the active region and acts as an amplifier. when both the emitter-base and collector-base junctions are foreward biased it operates in the saturation region and acts as closed switch. when the transistor is switched from cut-off to saturation and from saturation to cut-off with negligible active region, the transistor is operated as a switch. when the transistor is in saturation, junction voltages are very small but operating currents are large. when the transistor is in cut-off, the currents are zero (except the small leakage current) but the junction voltages are large.

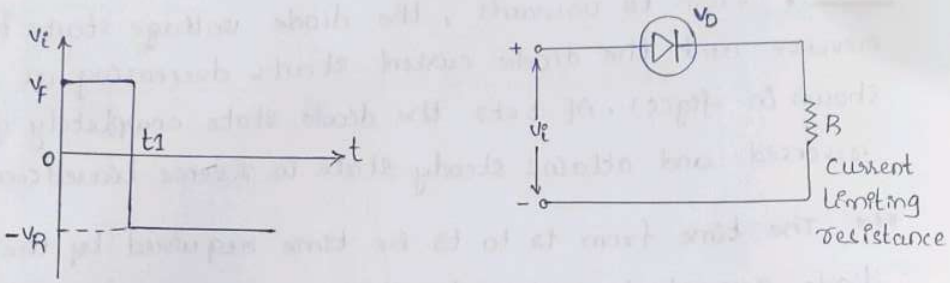
** To have fast switching from ON to OFF of a diode, the transition capacitance should be as small as possible.



Events during diode switching

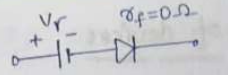
Diode switching times :

To analyze the various switching times, consider simple diode circuit and an input waveform shown below.

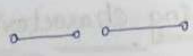


Event1 : Till time t_1, the forward voltage applied is V_F and diode is forward biased. The value of 'R' is large enough such that drop across forward biased diode is very small compared to drop across R. The forward current is then $I_F \approx V_F/R$, neglecting forward resistance of diode.

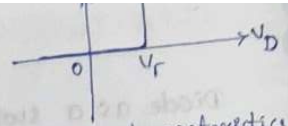
Event2 : At time t_1, the applied voltage is suddenly reversed and reverse voltage of $-V_R$ is applied to the circuit. Ideally diode also must become OFF from ON state instantly. But this does not happen instantly. The number of minority carriers takes time to reduce from $P_n - P_{no}$ to zero at the as shown in fig (b). due to this at t_1 current just reverses and remains at that reversed value $-I_R$ till the minority carrier concentration reduces to zero. This current is given by $-I_R = -V_R/R$. This continues to flow till time t_2.



(a) forward biased

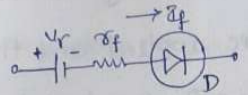


(b) Reverse biased

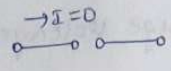


(c) V-I characteristics

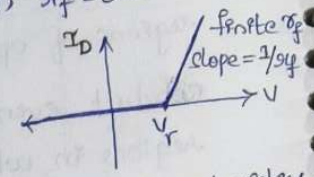
I. Linear piecewise model of diode with $r_f = 0\Omega$



(a) forward biased



(b) Reverse biased



(c) V-I characteristics

II. Linear piecewise model of diode with finite r_f

In the first approximation forward resistance is assumed to be "0Ω". In reverse biased, the diode is open circuit as shown in fig I(b). As diode conducts $V_D = V_r$, the V-I characteristics with straight lines is as shown in fig I(c).

As the method models the diode with the pieces of straight lines, the name given to such approximation is "piecewise-linear method". The characteristics of the diode is shown in the fig I(c) & fig II(c).

In the second approximation the r_f is considered to be finite, then in V-I characteristics, forward biased characteristics is a straight line with a slope equal to reciprocal of "r_f". In reverse bias the diode is assumed to be open circuited.

*** during time t_1 to t_2, the minority charge carriers remain stored and decrease slowly to zero. Hence this time is called "storage time" denoted as t_s.

Event3 : from t_2 onwards, the diode voltage starts to reverse and the diode current starts decreasing as shown in fig(c). At $t=t_3$ the diode state completely gets reversed and attains steady state in reverse biased condition.

*** The time from t_2 to t_3 i.e time required by the diode current to reduce to its reverse saturation value is called the "transition Interval" or "transition time" denoted as 't_t'.

[The total time required by the diode current to reduce to it's reverse saturation value is called the transiti]

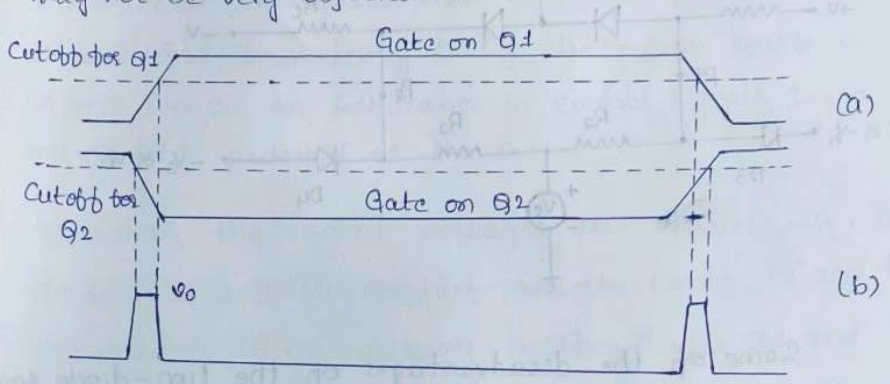
The total time required by the diode which is the sum of storage time and transition time to recover completely from the change of state is called "reverse recovery time" of the diode and denoted as 't_{rr}'. this is an important consideration in high speed switching applications.

** for quick switching from ON to OFF state, the recovery time should be as small as practicable.

$$t_{rr} = t_s + t_t$$

The reverse recovery time depends on the RC time constant where 'C' is a transition capacitance of a diode.

gate pulse is large compared with the active region base voltage range, so that each transistor, when it is not conducting is biased bas below cut-off. Then when the gate voltage appears, Q2 will be driven to cut-off before Q2 starts to conduct. Hence as a result of the gate signals themselves, the output appears as shown below figure. The gated signal voltage will appear super imposed on this waveform. If the gate waveform rise time is small compared with the gate duration, these spikes may not be very objectionable.



(a) The gating waveform drawn for with non-zero rise time

(b) Spikes which may occur in the output circuit of previous trig's -due to the gating waveform with non-zero rise time.

The circuit used to eliminate pedestal has the following drawbacks

(1) If the gating waveforms have definite rise and fall times, two sharp spikes are generated at the output.

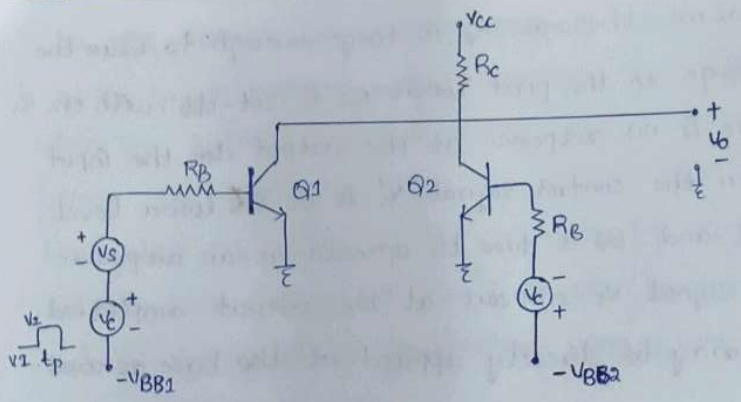


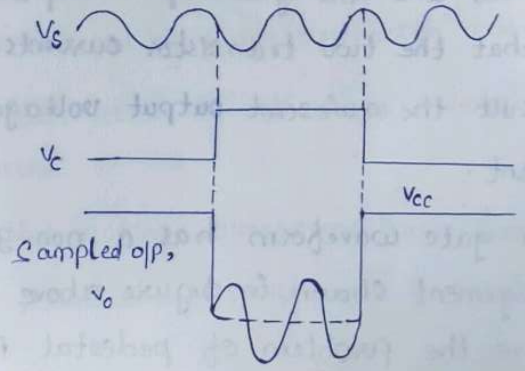
figure shows a symmetrical arrangement that suppresses the pedestal to a great extent. Q1 is the gating transistor and Q2 is used to minimize the pedestal. Gating voltages of opposite polarity are applied to the transistor bases. during the transmission time tp, when the control signal is at its upper level, Q1 conducts and Q2 is cut-off. A current flows from Vcc through Rc and Q1. during the non-transmission time when the control signal is at it's lower Level, Q1 is off and Q2 conducts and a current flows from Vcc through Rc and Q2. the base voltages $-V_{BB1}$ and $-V_{BB2}$ and the gate signal amplitude have been adjusted so that the two transistor currents are identical and as a result the quiescent output voltage level will remain constant.

If the gate waveform has a non-zero rise time then the arrangement shown in figure above does not completely solve the problem of pedestal. Assume that

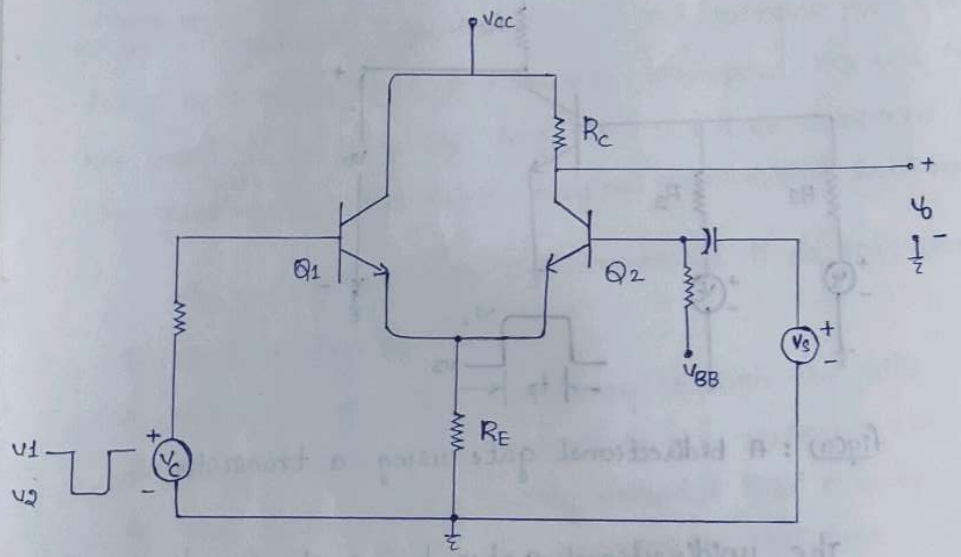
and the current through R_E is large enough to raise the emitter voltage to the point where Q2 is cut-off. With Q2 is cut-off there is no response at the output dos the input signal. When the control signal 'V_c' is at its lower level, Q1 is cutoff and Q2 is free to operate as an amplifier stage. The signal V_s appears at the output amplified. The signal may be directly applied at the base as well.

Reduction of pedestal in a gate circuit:

In the gate circuits previously discussed, initially the voltage level at the output is V_{cc}. When the gating signal is applied, the transistor draws current and the output therefore establishes itself at a new quiescent level. When a signal is applied, the output signal is superimposed on this new quiescent level. So the output during the gating interval appears as shown below figure, where the sampled portion of the signal is superimposed on a pedestal.



to the desired transmission interval. when the gating signal is at its lower level V_2, the transistor is well below cut-off. when the gating signal is at its upper level V_1, the bias brings the transistor into the active region. so as long as the gating signal is at its upper level, signals of either polarity appearing at the base will be sampled and will appear amplified at the output. Hence the circuit acts as a bidirectional gate.



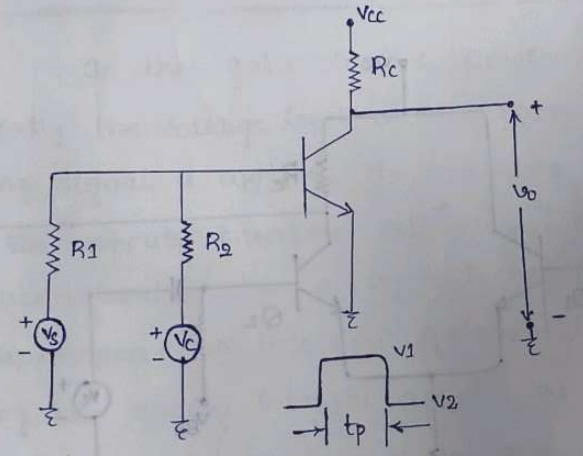
fig(b): Emitter coupled bidirectional sampling gate

figure shows a bidirectional gate using two transistors which are emitter coupled. In this, two separate bases are available for the signal and gating voltages. when the gate signal V_c is at its upper level, the transistor Q1 is ON

The disadvantages of the unidirectional gate are

1. There will be interaction between the signal source and the control voltage source.
2. The gate is of limited use because of the slow rise of the control voltage at the diode.

Bidirectional sampling gates using transistors:



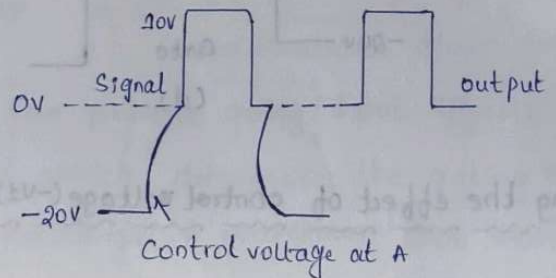
fig(a) : A bidirectional gate using a transistor

The unidirectional gates transmits signals of only one polarity, i.e either only positive signals or only negative signals. The signal voltage V_s and the control voltage V_c are applied through the summing resistors R1 and R2 to the base of a transistor. The gating voltage V_c is a pulse waveform between the levels v1 and v2 and with a pulse width tp equal

The input signal is a +10V pulse In fig(a), when the pulse has $-V_2 = -20V$ and $-V_1 = -10V$, there is no output pulse at all. In fig(b) when $-V_2 = -20V$ and $-V_1 = -5V$, the output is a +5V pulse. In fig(c) when $-V_2 = -20V$ and $-V_1 = 0V$, the output is a +10V pulse. In fig(d) when $-V_2 = -20V$ and $-V_1 = 5V$, the output is a 10V pulse superimposed on a pedestal of +5V. Actually the waveforms with vertical edges shown in figures (a), (b), (c), (d) are unrealistic because the RiCi network constitutes an integrating network for the gate waveform and therefore the gating signal will have exponentially rising and falling edges. Hence this type of gate is not suitable for transmi- shown in fig(e) -tting a portion of a continuous waveform. However if the input is a pulse of very short duration compared to the gate width, the input may be transmitted satisfactorily.

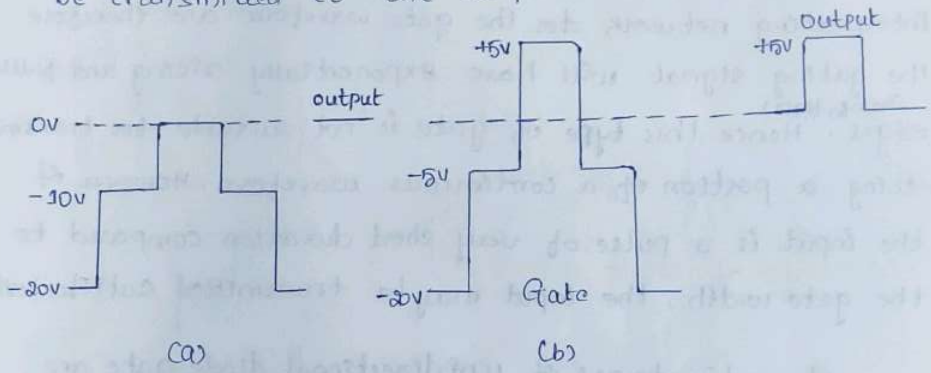
The advantages of unidirectional diode gate are

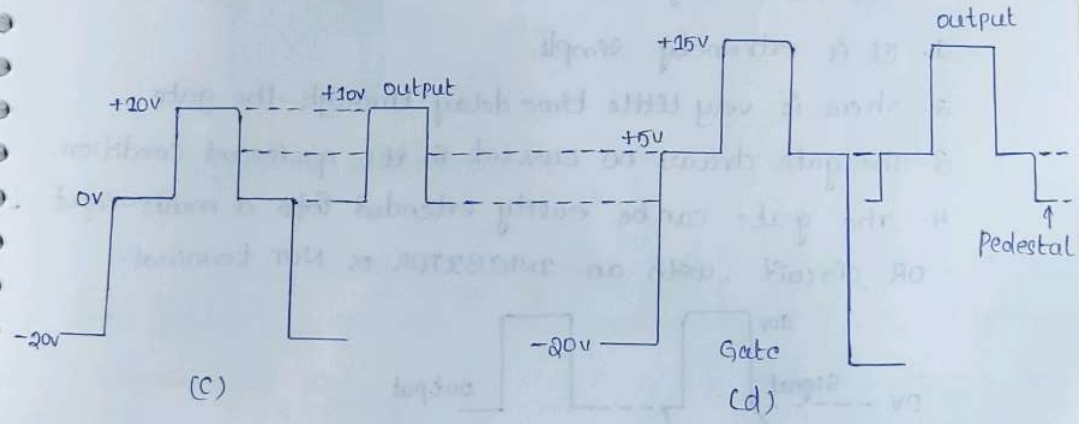
1. It is extremely simple
2. There is very little time delay through the gate.
3. The gate draws no current in its quiescent condition.
4. The gate can be easily extended into a multi-input OR circuit, with an INHIBITOR or NOT terminal.



(e) distortion of the control waveform

signal is called a control pulse, a selector pulse, or an enabling pulse. when the gating signal is at its lower level $-V_2$, the diode is heavily back biased and there will be no output to the input signal unless the peak amplitude of the input signal is larger than the magnitude of this back biasing voltage. when the gate signal is at it's upper level $-V_1$, a time coincident signal input pulse may be transmitted to the output.

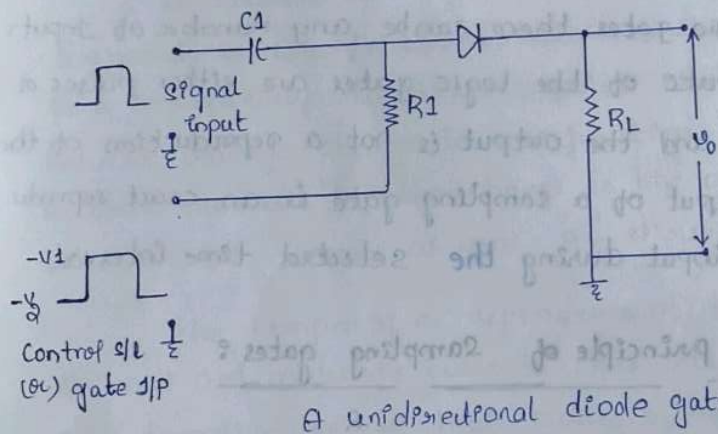




Illustrating the effect of control voltage ($-V_1$) on gate output

The basic operating principle of a sampling gate is illustrated in fig(a) & (b). In fig(a) the switch is normally open, but is in closed position when the signal is transmitted. In fig(b) the switch is normally closed, but is in open position when the signal is transmitted. These switches are normally electronic devices - diodes or transistors. when the device is conducting, it acts as a closed switch and when it is not conducting it acts as an open switch. Ideally a closed switch should have zero resistance and an open switch should have infinite resistance, but semiconductor devices do not have infinite back resistance and their forward resistances may lie in the range of several ohms.

Unidirectional diode gate:



A unidirectional diode gate which transmits only the positive going input signals. The gate signal i.e the signal which determines the gating or transmission period is a rectangular waveform that makes abrupt transition between the two negative levels $-V_1$ and $-V_2$. The gate

As Q1 cuts OFF, its collector voltage rises and when it reaches V, the "collector catching diode" D1 conducts and clamps the output to V.

Standard specifications:

In the cut-off region i.e for the off state

V_{BE} (cut-off) : $\leq$ 0V for silicon transistor

≤ -0.1 V for germanium transistor

In the saturation region, i.e for the ON state

V_{BE} (sat) : 0.7V for silicon transistor

0.3V for germanium transistor

V_{CE} (sat) : 0.3V for silicon transistor

0.1V for germanium transistor

The above values hold good for n-p-n transistors. for p-n-p transistors the above values with opposite sign are to be taken.

Test for saturation:

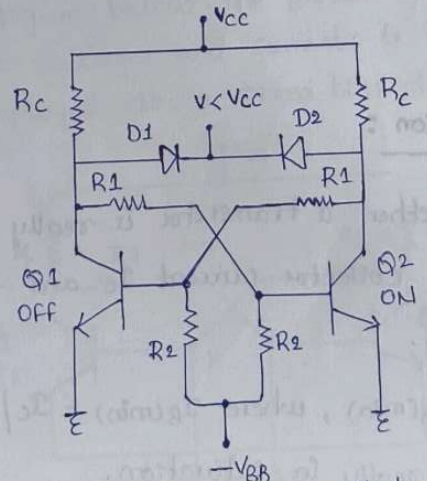
To test whether a transistor is really in saturation or not evaluate the collector current I_C and the base current I_B independently.

If $I_B > I_{B(min)}$, where $I_{B(min)} = I_C / h_{fe(min)}$ the transistor is really in saturation.

It is possible that Q2 may not be driven into saturation. Hence the flipflop circuit components must be chosen such that under the heaviest load, which the binary drives, one transistor remains in saturation while the other is in cut-off.

Since the resistor R1 also loads the off transistor to reduce loading, the value of R1 should be as large as possible compared to the value of R_c. But to ensure a loop gain in excess of unity during the transition between the states, R1 should be selected such that $R1 < h_{fe} R_c$.

For some applications, the loading varies with the operation being performed. In such cases, the extent to which a transistor is driven into saturation is variable. A constant output swing $V_w = V$, and a constant base saturation current I_{B2} can be obtained by clamping the collectors to an auxiliary voltage $V < V_{cc}$ through the diodes D1 and D2 as shown in figure below.



A fixed bias benary with collector catching diodes added

are consistent with the device characteristics and in which, in addition, the condition of the loop gain being less than unity is satisfied.

The condition with respect to loop gain will certainly be satisfied, if either of the two devices is below cut-off or if either device is in saturation. But normally the circuit is designed such that in a stable state one transistor is in saturation and the other one is in cut-off, because if one transistor is biased to be in cut-off and the other one to be in active region, as the temparature changes or the devices age and the device parameters vary, the quiescent point changes and the quiescent output voltage may also change appreciably. Sometimes the drift may be so much that the device operating in the active region may go into cut-off and with the devices in cut-off the circuit will be useless.

Loading:

The bistable multivibrator may be used to drive the other circuits and hence at one or both the collectors there are shunting loads, which are not shown in above figure. These loads reduce the magnitude of the collector voltage V_{C1} of the OFF transistor. This will result in reduction of the output voltage swing. A reduced V_{C1} will decrease I_{B2} and

and in the other stable states Q1 is OFF and Q2 is ON. Even-though the circuit is symmetrical, it is not possible for the circuit to remain in stable state with both the transistors conducting (i.e both operating in the active region) simultaneously and carrying equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents I_1 and I_2 and suppose there is a minute fluctuation in the current I_1, suppose it increases by a small amount then the voltage at the collector of Q1 decreases. This will results in a decrease in voltage at the base of Q2. So Q2 conducts less and I_2 decreases and hence the potential at the collector of Q2 increases. This results in an increase in the base potential of Q1. So Q1 conducts still more and I_1 is further increased and the potential at the collector of Q1 is further reduced and so on. [So the current I_1 is further increased and the potential at the collector] So the current I_1 keeps on increasing and the current I_2 keeps on decreasing till Q1 goes into saturation and Q2 goes into cut-off. This action keeps place because of the regenerative feedback incorporated into the circuit and will occur only if the loop gain is greater than one.

"A stable state of a binary is one in which the voltages and currents satisfy the Kirchoff's laws and

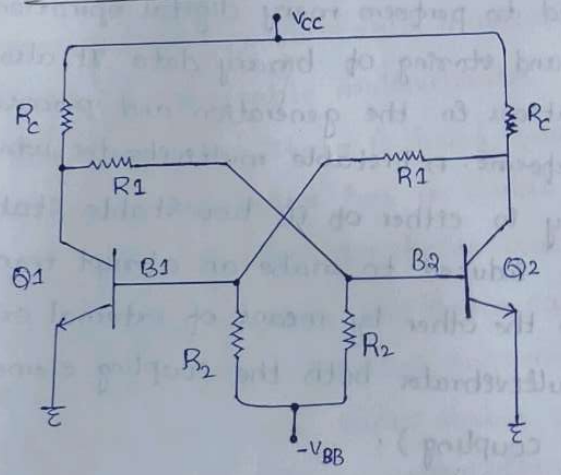
There are 2 types of Bistable multivebrators

1. collector coupled bistable multivebrator
2. Emitter coupled bistable multivebrator

There are two types of collector-coupled bistable multivebrators

1. fixed-bias bestable multivebrator.
2. self-bias bestable multivebrator.

Fixed-bias bestable multivebrator:



In the circuit shown above the output of each amplifier is direct coupled to the input of the other amplifier. In one of the stable states, transista Q1 is ON (i.e in Saturation) and Q2 is OFF (i.e in cut-off)

A monostable multivibrator requires a triggering signal to change from the stable state to the quasi stable state, but no triggering signal is required for the reverse transition i.e to bring it from the quasi stable state to the stable state. The astable multivibrator does not require any triggering at all. It keeps changing from one quasi stable state to another quasi stable state on its own the moment it is connected to the supply.

Bistable multivibrator:

A bistable multivibrator is the basic memory element. It is used to perform many digital operations such as counting and storing of binary data. It also finds extensive applications in the generation and processing of pulse type waveforms. A bistable multivibrator which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. In a bistable multivibrator both the coupling elements are resistors (dc coupling).

The bistable multivibrator is also called as multi, eccles-jordan circuit, trigger circuit, scale of-2 toggle circuit, flipflop and binary.